

g-byte Error Control Codes

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Abstract. This paper considers a model of error control codes for semiconductor memories consisting of RAM chips not necessarily of the same size. The data stored on a chip corresponds to a variable length byte and thus byte length is not same in this model and varies from chip to chip. The variable length byte is termed as a “general byte” or simply a “g-byte” [8]. The author in [8] has introduced and given the construction method of g-byte codes capable of correcting all single g-byte errors along with their decoding algorithm.

In this paper, we present three classes of g-byte codes, viz. the single g-byte error correcting codes with an alternative construction method of parity check matrix H , single error correcting and simultaneously single g-byte error detecting codes followed by sector error locating codes and single bit error correcting simultaneously with sector error locating g-byte codes.

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1. Introduction

Semiconductor memories used in existing computer systems and other digital devices have a byte-organized configuration [1-7, 15-19]. In this configuration, semiconductor memory system consists of “b-bit” organized memory RAM chips where $b = 4, 8, 16$ or 32 and all the RAM chips are of equal size. However, a more general and practical situation to consider is the setting where the RAM chips are not necessarily of the same size but have variable length. Keeping this in view, we consider the following more general configuration of semiconductor memories [8]:

Suppose the semiconductor memory consists of variable size RAM chips and those of the same size are adjacent to each other. The information stored on a chip corresponds to a byte of variable length depending on the size of the chip. Thus, the I/O data of a chip is termed as a “general byte” or simply a “g-byte”. The “g-bytes” are arranged in ascending order of their size. Also, g-bytes of the same size constitute a *sector*. An I/O word consists of “ s ” g-bytes of length $n_1, n_2, \dots, n_s$ resp. where $1 \leq n_1 \leq n_2 \leq \dots \leq n_s$ having total word length equal to $\sum_{j=1}^s n_j = n$ (say).

A practical situation is when semiconductor memories with g-byte arrangement are exposed to strong electromagnetic waves, radioactive particles or high energetic cosmic particles, then the errors caused due to a single hit results in the failure of a general RAM chip of g-byte length n_j for some j ($j = 1$ to s). Due to this failure of the chip, the resulting information read out from the memory is likely to have a single g-byte error where a *single g-byte error* is meant to be any number of errors confined to single g-byte.

Keeping this in view, the author in [8] has introduced and presented construction method of g-byte codes capable of correcting all single g-byte errors along with their decoding algorithm.

In this paper, we first present g-byte error control codes capable of correcting all single g-byte errors with an alternative construction method of parity check matrix H . We further consider another class of codes that are capable of correcting all single errors as well as can detect all single g-byte errors.

Finally, we present error location in g-byte error control codes where sector error locating g-byte codes and single bit error correcting simultaneously with sector error locating g-byte codes are discussed.

2. Definitions and Notations

Let $q = p^r$ be a prime or power of prime number. Let $\mathbf{F}_q$ be the finite field with q elements. Let $n_1, n_2, \dots, n_s$ be positive integers with $1 \leq n_1 \leq n_2 \leq \dots \leq n_s$. Let $n = \sum_{j=1}^s n_j$. Then we can write the field $\mathbf{F}_q^n$ as

$$\mathbf{F}_q^n = \mathbf{F}_q^{n_1} \oplus \mathbf{F}_q^{n_2} \oplus \dots \oplus \mathbf{F}_q^{n_s}.$$

Each vector $v \in \mathbf{F}_q^n = \oplus_{j=1}^s \mathbf{F}_q^{n_j}$ can be uniquely written as $v = (v_1, v_2, \dots, v_s)$ where $v_j \in \mathbf{F}_q^{n_j}$ for all $1 \leq j \leq s$. Here " v_j " is called the j^{th} g-byte of v .

Definition 2.1. Let $V \subseteq \mathbf{F}_q^n = \bigoplus_{j=1}^s \mathbf{F}_q^{n_j}$ be an $\mathbf{F}_q$ -subspace of vector space $\bigoplus_{j=1}^s \mathbf{F}_q^{n_j}$ equipped with the Hamming metric. Then V is called a *g-byte*

error control code denoted by $[n, k, d]$ where $n = \sum_{j=1}^s n_j$ = length of the code, $k = \dim_{\mathbf{F}_q} V$ and d = minimum distance of V .

Definition 2.2.

- (i) The generator matrix G of a $\left[\sum_{j=1}^s n_j, k, d \right]$ g-byte code is given as

$$G = [G_1 : G_2 : \dots : G_s],$$

where $G_j = (j = 1 \text{ to } s)$ is a $k \times n_j$ submatrix of G and is said to be the j^{th} g-byte of G of size n_j . The columns of j^{th} g-byte G_j of G are denoted as $g_{j,0}, g_{j,1}, \dots, g_{j,n_j-1}$ where $g_{j,l} \in \mathbf{F}_q^k$ for all $0 \leq l \leq n_j - 1$.

- (ii) The parity check matrix H of a $\left[\sum_{j=1}^s n_j, k, d \right]$ g-byte code is given as

$$H = [H_1 : H_2 : \dots : H_s],$$

where $H_j (j = 1 \text{ to } s)$ is a $R \times n_j$ (where $R = \sum_{j=1}^s n_j - k$) submatrix of H and is said to be the j^{th} g-byte of H of size n_j . The columns of H_j are denoted as $h_{j,0}, h_{j,1}, \dots, h_{j,n_j-1}$ where $h_{j,l} \in \mathbf{F}_q^R$ for all $0 \leq l \leq n_j - 1$.

Definition 2.3. A set of g-bytes viz. $\{H_{i_1}, H_{i_2}, \dots, H_{i_l}\} \subseteq \{H_1, H_2, \dots, H_s\}$ of the parity check matrix H is said to **linearly independent** over $\mathbf{F}_q$ if the union of all column vectors in the g-bytes $H_{i_1}, H_{i_2}, \dots, H_{i_l}$ is a linearly independent set over $\mathbf{F}_q$. Otherwise, we say that the set of g-bytes $H_{i_1}, H_{i_2}, \dots, H_{i_l}$ is linearly dependent.

Definition 2.4 [5]. Given a monic primitive polynomial $g(x)$ of degree r over $\mathbf{F}_q$, the $r \times r$ companion matrix M corresponding to $g(x)$ is defined as follows:

$$g(x) = g_0 + g_1x + g_2x^2 + \dots + g_{r-2}x^{r-2} + g_{r-1}x^{r-1} + x^r,$$

$$M = \begin{pmatrix} 0 & 0 & \dots & 0 & 0 & -g_0 \\ 1 & 0 & \dots & 0 & 0 & -g_1 \\ 0 & 1 & \dots & 0 & 0 & -g_2 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & \dots & 1 & 0 & -g_{r-2} \\ 0 & 0 & \dots & 0 & 1 & -g_{r-1} \end{pmatrix}_{r \times r}.$$

Observations.

- (i) Let α be a primitive element of $\mathbf{F}_q^r$ and a root of $g(x)$. Its companion

matrix M has its columns $\begin{pmatrix} \vdots \\ \vdots \\ \alpha^i \\ \vdots \\ \vdots \end{pmatrix}$ for $i = 1$ to r where $\begin{pmatrix} \vdots \\ \vdots \\ \alpha^i \\ \vdots \\ \vdots \end{pmatrix}$ is

the coefficient vector of $x^i \pmod{g(x)}$.

The companion matrix of α^j is M^j and its column vectors are expressed as follows:

$$M^j = \begin{pmatrix} \vdots & \vdots & \cdots & \vdots \\ \vdots & \vdots & \cdots & \vdots \\ \alpha^j & \alpha^{j+1} & \cdots & \alpha^{j+r-1} \\ \vdots & \vdots & \cdots & \vdots \\ \vdots & \vdots & \cdots & \vdots \end{pmatrix}_{r \times r}.$$

Let e be the exponent of $g(x)$, that is, $y = e$ is the least positive solution of $x^y \equiv 1 \pmod{g(x)}$. The companion matrix M has the following properties [5]:

- (a) M is non singular.
- (b) $M^0 = M^e = I_r$.
- (c) $M^i = M^j$ if and only if $i \equiv j \pmod{e}$.

Definition 2.5 [5]. Let r and t be positive integers with $t \leq r$. Let A be an $r \times r$ square matrix. The $r \times t$ *slimmed matrix* of A is obtained from A by keeping only the first t columns of A and deleting the last $r - t$ columns of A and is denoted as $[A]_t$.

3. Design of g-byte Error Correcting Codes

The author in [8] has given the construction method of g-byte codes capable of correcting all single g-byte errors. In this section, we present an alternative code construction method of g-byte error control codes correcting all single g-byte errors. We begin with the following result:

Theorem 3.1. An $[n, n-R, d]$ g-byte error correcting code where $n = \sum_{j=1}^s n_j$

satisfies the condition

$$R \geq \max_{j=1}^s \{n_i + n_j\}.$$

Proof. For a g-byte error correcting code, it is necessary and sufficient that any two g-bytes of the parity check matrix H are linearly independent over $\mathbf{F}_q$. For any two g-bytes say H_i and H_j , there exists $n_i + n_j$ column vectors and these column vectors should be linearly independent. Therefore the number of rows of the parity check matrix H should be at least $\max_{j=1}^s \{n_i + n_j\}$.

Example 3.2. Let $s = 3$, $q = 2$, $n_1 = 2$, $n_2 = 3$ and $n_3 = 4$. Let $r = 7$. Then $7 = r \geq \max_{i,j=1}^3 \{n_i + n_j\} = 7$.

Let

$$H' = [H_1 : H_2 : H_3],$$

with

$$H_1 = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix}, \quad H_2 = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix},$$

$$H_3 = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 1 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}.$$

Then H' is the parity check matrix of a g-byte error correcting code over $\mathbf{F}_2$ since any two g-bytes of H are linearly independent over $\mathbf{F}_2$.

Theorem 3.3. Let q, s be positive integers with q prime. Let $1 \leq n_1 \leq n_2 \leq \dots \leq n_s$ be the positive integers. Let $r \geq n_s$ be a positive integer such

that s divides $(q^r + 1)$. Let T be the $r \times r$ companion matrix of a monic primitive polynomial of degree r over $\mathbf{F}_q$. Let $[T]_{n_i}$ ($i = 1$ to s) be the $r \times n_i$ slimmed matrix of T and further, I_r and O_r are respectively the $r \times r$ identity and zero matrix over $\mathbf{F}_q$. Let $b = \left(\frac{q^r + 1}{s}\right)$. The code expressed by the following parity check matrix H is a single g -byte error correcting code having code length $N = \frac{(q^r + 1)}{s} (n_1 + n_2 + \cdots + n_s)$ and check bit length $R = 2r$:

$$H = [H_1 : H_2 : H_3 : \cdots : H_s],$$

where for $1 \leq j \leq s - 1$, the j^{th} sector H_j of length bn_j is given by

$$H_j = \begin{pmatrix} [I_r]_{n_j} & [I_r]_{n_j} & \cdots & \cdots & [I_r]_{n_j} \\ [T^{(j-1)b}]_{n_j} & [T^{(j-1)b+1}]_{n_j} & \cdots & \cdots & [T^{jb-1}]_{n_j} \end{pmatrix}_{2r \times bn_j},$$

and

$$H_s = \begin{pmatrix} [I_r]_{n_s} & [I_r]_{n_s} & \cdots & \cdots & [I_r]_{n_s} & [I_r]_{n_s} & [O_r]_{n_s} \\ [T^{(s-1)b}]_{n_s} & [T^{(s-1)b+1}]_{n_s} & \cdots & \cdots & [T^{sb-3}]_{n_s} & [O_r]_{n_s} & [I_r]_{n_s} \end{pmatrix}_{2r \times bn_s}.$$

Proof. Proof follows from the fact that any two g -bytes of H are linearly independent over $\mathbf{F}_q$.

Example 3.4. Let $s = 3$, $q = 2$, $n_1 = 2$, $n_2 = 3$ and $n_3 = 4$. Then $r = 5$ is the least positive integer such that $s = 3$ divides $q^r + 1 = 2^5 + 1 = 33$. Here $b = \frac{q^r + 1}{s} = \frac{33}{3} = 11$.

Thus each sector H_j ($j = 1$ to s) of the parity check matrix H consists of 11 g -bytes each of length n_j . Let T be a 5×5 companion matrix over $\mathbf{F}_2$. Then

$$H = (A \quad \cdots \quad B)$$

where

$$A = \begin{pmatrix} [I_5]_2 & [I_5]_2 & \cdots & [I_5]_2 & \vdots & [I_5]_3 & [I_5]_3 & \cdots \\ [T^0]_2 & [T^1]_2 & \cdots & [T^{10}]_2 & \vdots & [T^{11}]_3 & [T^{12}]_3 & \cdots \end{pmatrix},$$

$$B = \begin{pmatrix} \cdots & [I_5]_3 & \vdots & [I_5]_4 & \cdots & [I_5]_4 & [I_5]_4 & [O_5]_4 \\ \cdots & [T^{21}]_3 & \vdots & [T^{22}]_4 & \cdots & [T^{30}]_4 & [O_5]_4 & [I_5]_4 \end{pmatrix}$$

is the parity check matrix of a g-byte error correcting code having code length $N = 99$ and check bit length $R = 10$.

Note that the monic primitive polynomial of degree 5 over $\mathbf{F}_2$ is given by $x^5 + x^2 + 1$ and the corresponding 5×5 companion matrix T over $\mathbf{F}_2$ is given by:

$$T = \begin{pmatrix} 0 & 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \end{pmatrix}_{5 \times 5}.$$

Example 3.5. Let $s = 3$, $q = 2$, $n_1 = 1$, $n_2 = 2$ and $n_3 = 3$. Then $r = 3$ is the least positive integer such that $s = 3$ divides $q^r + 1 = 2^3 + 1 = 9$. Let T be the 3×3 companion matrix corresponding to the monic primitive polynomial $x^3 + x + 1$ over $\mathbf{F}_2$. Then various powers of T are given by

$$\begin{aligned} T^0 &= \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{pmatrix}, & T^1 &= \begin{pmatrix} 0 & 0 & 1 \\ 1 & 0 & 1 \\ 0 & 1 & 0 \end{pmatrix}, \\ T^2 &= \begin{pmatrix} 0 & 1 & 0 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \end{pmatrix}, & T^3 &= \begin{pmatrix} 1 & 0 & 1 \\ 1 & 1 & 1 \\ 0 & 1 & 1 \end{pmatrix}, \\ T^4 &= \begin{pmatrix} 0 & 1 & 1 \\ 1 & 1 & 0 \\ 1 & 1 & 1 \end{pmatrix}, & T^5 &= \begin{pmatrix} 1 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 1 & 0 \end{pmatrix}, \\ T^6 &= \begin{pmatrix} 1 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{pmatrix}, & T^7 &= I_3 = T^0. \end{aligned}$$

Here $b = \frac{q^r + 1}{s} = \frac{2^3 + 1}{3} = 3$.

The parity check matrix H given by:

$$H = \begin{pmatrix} [I_3]_1 & [I_3]_1 & [I_3]_1 & \vdots & [I_3]_2 & [I_3]_2 & [I_3]_2 & \vdots & [I_3]_3 & [I_3]_3 & [O_3]_3 \\ [T^0]_1 & [T^1]_1 & [T^2]_1 & \vdots & [T^3]_2 & [T^4]_2 & [T^5]_2 & \vdots & [T^6]_3 & [O_3]_3 & [I_3]_3 \end{pmatrix}$$

$$= \begin{bmatrix} 1 & 1 & 1 & \vdots & 10 & 10 & 10 & \vdots & 100 & 100 & 000 \\ 0 & 0 & 0 & \vdots & 01 & 01 & 01 & \vdots & 010 & 010 & 000 \\ 0 & 0 & 0 & \vdots & 00 & 00 & 00 & \vdots & 001 & 001 & 000 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ 1 & 0 & 0 & \vdots & 10 & 01 & 11 & \vdots & 110 & 000 & 100 \\ 0 & 1 & 0 & \vdots & 11 & 11 & 10 & \vdots & 001 & 000 & 010 \\ 0 & 0 & 1 & \vdots & 01 & 11 & 11 & \vdots & 100 & 000 & 001 \end{bmatrix}_{6 \times 18}$$

is the parity check matrix of a g-byte error correcting code having code length $N = 99$ and check bit length $R = 6$.

4. SEC-S_{g-byte} ED codes

In this section, we present another class of g-byte error control codes capable of correcting all single bit errors and simultaneously detecting all single g-byte errors.

Theorem 4.1. Let $1 \leq n_1 \leq n_2 \leq n_3 \leq \dots \leq n_s$ be s positive integers. Let $R \geq 2n_s$. Let H be the $R \times (q^{R-n_i} - 1)n_i$ matrix given by

$$H = [H_1, H_2, \dots, H_s],$$

where for $1 \leq i \leq s$, H_i is given by

$$H_i = \begin{bmatrix} M_{i,1} & M_{i,2} & \dots & M_{i,J_i} \\ I_{n_i} & I_{n_i} & \dots & I_{n_i} \end{bmatrix}_{R \times (q^{R-n_i}-1)n_i},$$

and $J_i = (q^{R-n_i} - 1)$, $M_{i,k} = (R - n_i) \times n_i$ matrix whose columns are the n_i -copies of the q -ary representation of the integer k for $1 \leq k \leq J_i$ and

I_{n_i} is the $n_i \times n_i$ identity matrix. The code which is the null space of H is a single error correcting and simultaneously single g-byte error detecting (SEC-S_{g-byte} ED) code having code length $N = \sum_{i=1}^s (q^{R-n_i} - 1)n_i$ consisting of s sectors and the i^{th} sector ($1 \leq i \leq s$) consist of $(q^{R-n_i} - 1)$ g-bytes of size n_i each.

Proof. Let

E_1 = Error set consisting of all single bit errors; and

E_2 = error set consisting of all single g-byte errors excluding single bit errors.

In order to show that the linear code which is the null space of H corrects all errors in E_1 and simultaneously detects all errors in E_2 , it suffices to show that

- (i) $EH^T \neq 0$ for all $E \in \{E_1 \cup E_2\}$,
- (ii) $E_i H^T \neq E_j H^T$ for all $E_i, E_j \in E_1, E_i \neq E_j$,
- (iii) $E_i H^T \neq E_k H^T$ for all $E_i \in E_1$ and for all $E_k \in E_2$.

Now, we prove (i), (ii) and (iii).

(i) It clearly holds.

(ii) Let $E_i, E_j \in E_1, E_i \neq E_j$.

Clearly if E_i and E_j are occurring in g-bytes of different sectors, then $E_i H^T \neq E_j H^T$. However, if E_i and E_j occur in g-bytes of the same sector, then also $E_i H^T \neq E_j H^T$.

(iii) Clearly, $E_i H^T \neq E_k H^T$ for all $E_i \in E_1$ and for all $E_k \in E_2$.

Hence the proof. □

Example 4.2. Let $s = 2, q = 2, n_1 = 2$ and $n_2 = 3$. Let $R = 6$. Then $J_1 = q^{R-n_1} - 1 = 2^4 - 1 = 15$, $J_2 = q^{R-n_2} - 1 = 2^3 - 1 = 7$.

Let $H = [H_1 \ H_2]$ where

$$H_1 = \begin{bmatrix} 11 & 00 & 11 & 00 & 11 & 00 & 11 & 11 & 00 & 11 & 00 & 11 & 00 & 11 \\ 00 & 11 & 11 & 00 & 00 & 11 & 11 & 00 & 11 & 11 & 00 & 00 & 11 & 11 \\ 00 & 00 & 00 & 11 & 11 & 11 & 11 & 00 & 00 & 00 & 11 & 11 & 11 & 11 \\ 00 & 00 & 00 & 00 & 00 & 00 & 00 & 11 & 11 & 11 & 11 & 11 & 11 & 11 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ 10 & 10 & 10 & 10 & 10 & 10 & 10 & 10 & 10 & 10 & 10 & 10 & 10 & 10 \\ 01 & 01 & 01 & 01 & 01 & 01 & 01 & 01 & 01 & 01 & 01 & 01 & 01 & 01 \end{bmatrix}_{6 \times 30},$$

$$H_2 = \begin{bmatrix} 111 & 000 & 111 & 000 & 111 & 000 & 111 \\ 000 & 111 & 111 & 000 & 000 & 111 & 111 \\ 000 & 000 & 000 & 111 & 111 & 111 & 111 \\ \dots & \dots & \dots & \dots & \dots & \dots & \dots \\ 100 & 100 & 100 & 100 & 100 & 100 & 100 \\ 010 & 010 & 010 & 010 & 010 & 010 & 010 \\ 001 & 001 & 001 & 001 & 001 & 001 & 001 \end{bmatrix}_{6 \times 21}.$$

Then the null space of H is a single g-byte error correcting and simultaneously single g-byte error detecting code with code length $N = 51$ and number of parity check digits $R = 6$. The codewords consist of 2 sectors. The first sector consists of 15 g-bytes each of length 2-bits and the second sector consists of 7 g-bytes each of length 3-bits.

5. Error Location in g-byte Codes

The technique of error location lies midway between error correction and error detection. The codes firstly presented in this section are capable of locating an erroneous sector that contains a single g-byte error. We call these codes as “g-sector error locating codes” or $S_{p/(l_i \times m_i)}$ error locating codes where $\sum_{i=1}^p = s$ and $\sum_{j=1}^s = n$.

Further, the predominant errors in g-byte organised semiconductor memory chips caused by α -particles and external noises occur as single bit errors. Therefore, an error locating code capable of correcting single bit errors is very useful.

Keeping this in view, we also discuss single bit error correcting and g-sector error locating codes (i.e. SEC- $S_{p/(l_i \times m_i)}$ error locating codes) or equivalently, g-sector error locating codes with single-bit error correction capability. Once the faulty g-sector is located by a code, then the faulty sector can be replaced by a correct one and the system can be recovered and proceed with normal operations.

5.1. g-Sector error locating ($S_{p/(l_i \times m_i)}$) EL-codes

In this subsection, we define a class of g-sector error locating codes that can locate an erroneous g-sector containing a single g-byte error. Such codes are denoted as $S_{p/(l_i \times m_i)}$ EL codes. The $S_{p/(l_i \times m_i)}$ EL codes locate a single g-byte within a g-sector.

Theorem 5.1. *Let $1 \leq n_1 \leq n_2 \leq \dots \leq n_s$ be positive integers and R be a positive integer such that $R \geq \max_{i,j=1}^p \{l_1 + l_j\}$. Let H' be the $R \times \sum_{i=1}^p l_i n_i$ parity check matrix of a g-byte error correcting code given by*

$$H' = \begin{bmatrix} \underbrace{H_1}_{m_1} & \underbrace{H_2}_{m_2} & \dots & \underbrace{H_s}_{m_p} \end{bmatrix}_{R \times \sum_{i=1}^p l_i n_i},$$

where any two g-bytes of H' are linearly independent over $\mathbf{F}_q$.

Then the code described by the following matrix H is an $S_{p/(l_i \times m_i)}$ EL-code:

$$\begin{aligned} H &= \begin{bmatrix} \underbrace{H_1 \ H_1 \ \dots \ H_1}_{l_1 \text{ g-bytes}} & \vdots & \underbrace{H_2 \ H_2 \ \dots \ H_2}_{l_2 \text{ g-bytes}} & \vdots & \dots & \vdots & \underbrace{H_s \ H_s \ \dots \ H_s}_{l_p \text{ g-bytes}} \end{bmatrix}_{R \times ps}, \\ &= \begin{bmatrix} \underbrace{H_1 \ H_1 \ \dots \ H_1}_{l_1 m_1 \text{-bits}} & \vdots & \underbrace{H_2 \ H_2 \ \dots \ H_2}_{l_2 m_2 \text{-bits}} & \vdots & \dots & \vdots & \underbrace{H_s \ H_s \ \dots \ H_s}_{l_p m_p \text{-bits}} \end{bmatrix}_{R \times ps}. \end{aligned}$$

(Note that here each codeword consists of p sectors having lengths $l_1 m_1$,

$l_2 m_2 \cdots l_p m_p$ resp. The i^{th} *g*-sector $G - i$ ($1 \leq i \leq p$) consists of l_i *g*-bytes each of size m_i -bits.)

Proof. The theorem can be easily proved because parity check matrix of the $S_{p/(l_i \times m_i)}$ EL-codes is organised by l_i repetition of H_i in the i^{th} *g*-sector for $1 = 1, 2, \dots, p$ and any two *g*-bytes occurring in different sectors are linearly independent over $\mathbf{F}_q$. $\square$

Example 5.2. Let $q = 2, p = 3, l_1 = 2, l_2 = 3, l_3 = 4, m_1 = 6, m_2 = 4$ and $m_3 = 3$. Consider the parity check matrix $H' = [H_1 \vdots H_2 \vdots H_3]$ given in Example 3.2 with $R = r = 7$.

The parity check matrix H given by

$$H = \left[\begin{array}{cccccc} \underbrace{H_1 \ H_1 \ H_1 \ H_1 \ H_1 \ H_1}_{6 \text{ g-bytes}} & \underbrace{H_2 \ H_2 \ H_2 \ H_2}_{4 \text{ g-bytes}} & \underbrace{H_3 \ H_3 \ H_3}_{3 \text{ g-bytes}} \end{array} \right]_{7 \times 36}$$

describes an $S_{12/(12 \times 3)}$ EL code organized in three sectors. The first *g*-sector viz. G_1 , sector consists of 6 *g*-bytes each of length 2. The second sector viz. g_2 consists of 4 *g*-bytes each of length 3 and the third sector viz. G_3 sector consists of 3 *g*-bytes each of length 4.

5.2. Single bit error correcting and single sector error locating (SEC- $S_{p/(l_i \times n_i)}$ EL) codes

This subsection deals with the SEC- $S_{p/(l_i \times n_i)}$ EL-codes that correct single-bit errors and locate a *g*-byte error within a *g*-sector.

5.2.1. Code conditions and bounds

Let E_s be the error set of errors of length $1 \times ps$ (where $p = lcm(n_1, n_2, \dots, n_s)$) consisting of all single-bit errors. Let $E_i(E_j)$ be the error set consisting of all single *g*-byte errors occurring in the $i^{th}(j^{th})$ -*g*-sector excluding single bit errors. Thus, $E_i \cap E_s = E_j \cap E_s = \phi$ for all $i \neq j$. The following theorem

describes the necessary and sufficient condition that characterizes single bit error correcting and single sector locating (SEC- $S_{p/(l_i \times n_i)}$ EL-codes.

Theorem 5.3. *A linear g-byte code described by the parity check matrix H corrects all errors in E_s and locates all errors in E_i or E_j where $i \neq j$ iff*

- (i) $EH^T \neq 0$ for all $E \in \{E_s \cup E_i \cup E_j\}$.
- (ii) $E_1H^T \neq E_2H^T$ for all $E_1, E_2 \in E_s, E_1 \neq E_2$.
- (iii) $E_3H^T \neq E_4H^T$ for all $E_3 \in E_i$ and for all $E_4 \in E_j$.
- (iv) $E_1H^T \neq E_3H^T$ for all $E_1 \in E_s$ and for all $E_3 \in E_i$.

Proof. It is apparent that conditions (i) and (ii) are necessary conditions for correcting all single bit errors. Conditions (i) and (iii) are necessary conditions for indicating the location of an erroneous g-sector containing single g-byte errors. Conditions (i) and (iv) are necessary conditions for distinguishing single bit errors from a single g-byte error (excluding single bit errors) occurring in a sector. So the SEC- $S_{p/(l_i \times n_i)}$ EL-codes must satisfy all the conditions (i) to (iv).

Conversely, if a code satisfies conditions (i) to (iv), then we can distinguish single bit errors from single g-byte errors. We can also correct all single bit errors and locate all single g-byte errors within a sector. Therefore, this code is an SEC- $S_{p/(l_i \times n_i)}$ EL-code. $\square$

Theorem 5.4. *Let $1 \leq n_1, \leq n_2, \dots, \leq n_s$ positive integers. Let $p = \text{lcm}(n_1, n_2, \dots, n_s)$. Let there be p g-sectors viz. $G_1, G_2, \dots, G_p$ where i^{th} g-sector G_i consists of m_i g-bytes of length l_i . Then an $(N, N - R)$ SEC- $S_{p/(l_i \times m_i)}$ EL-code over $\mathbf{F}_q$ where $N = \sum_{i=1}^p l_i m_i$ consisting of p g-sectors and i^{th} g-sector ($1 \leq i \leq p$) consists of m_i g-bytes each of size l_i must*

satisfy the following condition:

$$q^R - 1 \geq \sum_{i=1}^p [l_i(m_i - 1) + q_i^{l_i}] - p.$$

Proof. In the SEC- $S_{p/(l_i \times m_i)}$ EL-code, in general, the syndromes caused by single bit errors should be different from each other. Also, the errors caused by single g-byte errors (excluding single bit errors) occurring within a g-sector should have different syndromes from the ones caused by single bit errors. Therefore, the errors in the i^{th} g-sector ($1 \leq i \leq p$) have at least $p + [(q^{n_i} - 1) - n_i]$ different syndromes and hence there are at least

$$\begin{aligned} & \sum_{i=1}^p l_i m_i + [(q_i^{l_i} - 1) - l_i] \\ &= \sum_{i=1}^p l_i (m_i - 1) + q^{l_i} - p \end{aligned}$$

different syndromes in the received word.

Hence the following inequality is satisfied:

$$q^R - 1 \geq \sum_{i=1}^p l_i (m_i - 1) + q^{l_i} - p.$$

6. Conclusion

g-byte error correcting codes have been introduced by the author in [8]. In this paper, we first presented single g-byte error correcting codes with an alternative approach followed by single error correcting and simultaneously g-byte error detecting codes. Finally, we discussed error location in g-bytes error control codes by way of presenting sector error locating g-byte codes and single bit error correcting simultaneously with sector error locating g-byte codes.

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